REMARKS/ARGUMENTS

This is in response to the Office Action of March 20, 2006.

Claims 1 through 16, 19 through 24, 26 through 41, and 44 through 49 are currently pending in the application.

Claims 1 through 16, 19 through 24, 26 through 41, and 44 through 49 stand rejected.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,864,178 to Yamada et al. in view of U.S. Patent No. 4,231,910 to Plueddemann

Claims 1 through 16, 19 through 24, 26 through 41, and 44 through 49 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamada et al. (U.S. Patent 5,864,178) in view of Plueddemann (U.S. Patent 4,231,910). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Turning to the cited prior art Yamada et al. reference, teaches or suggests a semiconductor device comprising a wiring circuit board and a semiconductor chip mounted through a bump electrode on the circuit board, a space between the circuit board and the semiconductor chip as well as a periphery of the semiconductor chip being encapsulated with a resin containing filler. In FIGS. 56A through 56D a semiconductor chip 201 is mounted on a wiring circuit board 202 using bumps 203 with the semiconductor chip 201 having a layer of a

first resin 204 constituting a laminate of encapsulation resin, a second layer of resin 205 on the wiring circuit board 202 constituting a laminate of encapsulation resin, a third encapsulation resin 206 constituting a laminate of encapsulation resin applied to a portion of the second layer of resin 205, a polymer film 207 formed on the semiconductor chip 201, and a polymer film 208 formed on the wiring circuit board 202. A passivation film 223 is formed on polymer film 208 which is excellent in wettability with the encapsulation resin, such as a hydrocarbon wax, a fatty acid type wax, a fatty amide type wax or an ester type wax. For example, an ester type wax such as carnauba wax or montan wax is preferable in view of their excellent moisture resistance. Other examples useful in Example VIII are a long chin carboxylic acid or a metal salt thereof, such as stearic acid, palmitic acid, zinc stearate and calcium stearate; and a low molecular polyethyleme wax which may be applied singly or in combination thereof. Nowhere does Yamada et al. teach or suggest a semiconductor chip 201 having at least a portion of said active surface having a wetting agent layer of about a monolayer thick thereon, said wetting agent layer wetable by a polymeric material. At best, Yamada et al. describe that solely the first layer of encapsulation resin 204, second layer of encapsulation resin 205, and third encapsulation resin 206 may include a silane coupling agent therein mixed with the other components forming the layer of encapsulation resin. The silane coupling agent is only used in the formulation of the encapsulation resin itself, not separately applied to either the semiconductor chip or the wiring circuit board as a wetting agent layer. Nowhere in the Yamada et al. reference is there any description whatsoever directed to any of the encapsulation resins 204, 205, and 206 acting as a wetting agent under any circumstances.

Plueddemann teaches a primer composition for improving adhesion between a solid substrate and a thermosetting resins. In the description of the invention, the composition consists essentially of 1 to 25 weight percent of an organosilicon compound selected from a group of silane compounds or partial hydrolyzates thereof and 75 to 99 weight percent of an alkoxymethyltriazine (see col. 2, lines 5-17). Plueddemann teaches an improved wet and dry adhesion of thermoplastics to solid substrates. (see col. 3, lines 22-24). The primer compound of Plueddemann is not directed to improved flow of an underfill material. Plueddemann does not teach or suggest the use of a wetting agent whatsoever.

For instance, Applicant asserts that the any combination of the Yamada et al. reference and the Plueddemann reference does not teach or suggest the claim limitations of the claimed inventions set forth in independent claims 1, 6, 10, 14, 20, 23, 26, 31, 35, 39, 45, and 48 calling for "the semiconductor device having an active surface, at least a portion of said active surface having a wetting agent layer of about a monolayer thickness thereon comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during a curing process for a material", "a wetting agent layer provided on said active surface of said semiconductor device, said wetting agent layer having a thickness of about a monolayer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during a curing process for a material", "a wetting agent located on a portion of said active surface of said semiconductor device comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during a curing process for a material", "a wetting agent layer provided on at least a portion of said active surface of said semiconductor device comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during a curing process for a material, the underfill material essentially filling a volume between said wetting agent layer and said upper surface of said substrate", "a wetting agent layer provided on a portion of said active surface of said semiconductor device and a portion of said upper surface of said substrate, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during a curing process for a material", "a wetting agent layer provided on said active surface of said semiconductor device and on said upper surface of said substrate, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during a curing process for a material", "the semiconductor die having an active surface, at least a portion of said active surface having a wetting agent layer of about a monolayer in thickness thereon, said wetting agent layer wetable by a polymeric material, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during a curing process for a material", "a wetting agent layer provided on said active surface of said semiconductor die, said wetting agent layer having a thickness of

about a monolayer and wetable by a polymeric material, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during a curing process for a material", "a wetting agent layer provided on a portion of said active surface of said semiconductor die and a portion of said upper surface of said substrate, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during a curing process for a material", and "a wetting agent layer provided on said active surface of said semiconductor die and on said upper surface of said substrate, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during a curing process for a material".

In contrast to the claimed inventions, Applicant asserts that nowhere does the combination of the Yamada et al. reference and the Plueddemann reference teaches or suggests a wetting agent used on a portion of a semiconductor device, semiconductor die, or substrate in any manner. At best, the Yamada et al. reference discusses the use of silane coupling agent mixed with the other components forming the layer of encapsulation resin. The silane coupling agent is only used in the formulation of the encapsulation resin itself, not separately applied to either the semiconductor chip or the wiring circuit board. At best, the Plueddemann reference teaches or suggests the use a primer composition for improving adhesion between a solid substrate and thermosetting resins. There is no teaching or suggestion whatsoever in the Plueddemann reference regarding the use of the primer composition as a wetting agent. Applicants assert that the Plueddemann reference contains no teaching or suggestion whatsoever for the use of the primer agent with an encapsulation layer such as contained in the Yamada et al. reference. The claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45, and 48 are not directed to the use of a silane coupling agent in the formulation of an encapsulation resin or a primer agent applied to the surface of an encapsulation resin containing a silane coupling agent in the formulation thereof. Therefore, any combination of the Yamada et al. reference and the Plueddemann reference cannot and does establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 26, 31, 35, 39, 45, and 48. Accordingly, independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45, and 48 are allowable as well as the dependent claims therefrom.

Further, Applicant asserts that any combination of the Yamada et al. reference and the Plueddemann reference is a hindsight reconstruction of the Applicant's claimed inventions by picking and choosing among the cited prior art based solely upon Applicant's disclosure because the cited prior art fails to suggest any reason for any combination thereof and, even if combined, does not teach or suggest the claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45, and 48. Such hindsight is evidenced by the attempted modification of the Yamada et al. reference to include the use of a primer agent for adhesion purposes. The Yamada et al. reference needs no primer agent for adhesion purposes and does not teach or suggest the use of one in any manner. Therefore, any combination of the Yamada et al. reference and the Plueddemann reference cannot and does establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 26, 31, 35, 39, 45, and 48. Accordingly, independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45, and 48 are allowable as well as the dependent claims therefrom.

CONCLUSION

Claims 1 through 16, 19 through 24, 26 through 41, and 44 through 49 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,

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